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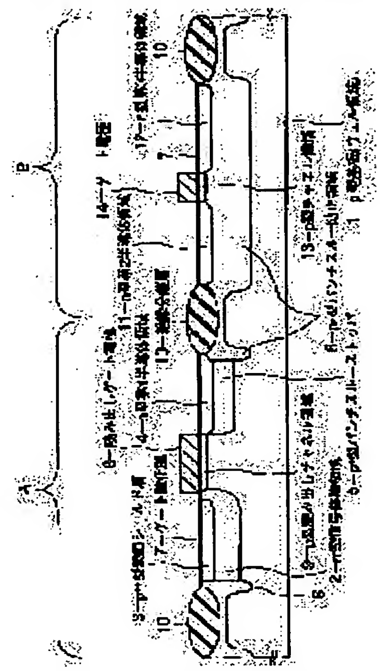
(54) MOS-TYPE SOLID-STATE IMAGE PICKUP DEVICE AND METHOD OF MANUFACTURING THE SAME

(57)Abstract:
PROBLEM TO BE SOLVED: To realize improved charge transfer performance and prevention of punch-through at the same time, even if a MOS element is shrunk in size, in a MOS-type solid-state image pickup device.
SOLUTION: A p+ type punch-through preventing region 6 is not formed in a region directly under an n- type signal accumulation region 2 of a photodiode. The n- type signal accumulating region 2 is formed inside a p type semiconductor substrate 1. The p+ type punch-through preventing region 6 is formed over the entire part of an element region B, which is a region other than an element region A, where the photodiode and a read gate are formed. To prevent punch-through effect between elements, the p+ type punch-through preventing region 6 is also formed directly under an insulation separation layer 10. A p+ type punch-through stopper 5 may be formed directly under an n type first semiconductor region 4.



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CLAIMS

[Claim(s)]

[Claim 1] The 1st MOS transistor of the 2nd conductivity type for reading the optoelectric transducer formed in the semi-conductor substrate of the 1st conductivity type, and the charge which is formed in the 1st element field of said semi-conductor substrate, and is generated by said optoelectric transducer, The MOS mold solid state camera characterized by providing the 2nd MOS transistor of the 2nd conductivity type formed in the 2nd element field of said semi-conductor substrate, and establishing the punch-through prevention field of the 1st conductivity type for preventing a punch-through in said whole 2nd element field.

[Claim 2] It is the MOS mold solid state camera according to claim 1 which possesses the discrete insulating layer which encloses said the 1st and 2nd element field, and is characterized by preparing said punch-through prevention field also directly under said discrete insulating layer.

[Claim 3] Said punch-through prevention field is an MOS mold solid state camera according to claim 2 characterized by being prepared in the periphery of said 1st element field along with said discrete insulating layer.

[Claim 4] The width of face from said discrete insulating layer to the edge of said punch-through prevention field in said 1st element field is an MOS mold solid state camera according to claim 3 characterized by being secured more than a doubling gap of the mask material used in case said punch-through prevention field is formed.

[Claim 5] Said width of face is an MOS mold solid state camera according to claim 4 characterized by being 0.2 micrometers or more.

[Claim 6] The location of said punch-through prevention field in said 2nd element field is an MOS mold solid state camera according to claim 2 characterized by being deeper than the location of said punch-through prevention field in directly under [of said discrete insulating layer].

[Claim 7] It is the MOS mold solid state camera according to claim 1 which said MOS mold solid state camera has two or more pixels, and is characterized by each pixel having said optoelectric transducer, said 1st MOS transistor, and said 2nd MOS transistor.

[Claim 8] Said optoelectric transducer is an MOS mold solid state camera according to claim 1 characterized by being formed in said 1st element field and the source of said 1st MOS transistor serving as a signal are recording field of the 2nd conductivity type of said optoelectric transducer.

[Claim 9] The MOS mold solid state camera according to claim 8 characterized by providing the punch-through stopper of the 1st conductivity type formed directly under the drain of said 1st MOS transistor.

[Claim 10] Said punch-through prevention field is an MOS mold solid state camera according to claim 8 characterized by being prepared directly under the drain of said 1st MOS transistor.

[Claim 11] Said punch-through prevention field is an MOS mold solid state camera according to claim 8 characterized by having covered the drain of said 1st MOS transistor, and a part of channel.

[Claim 12] Said optoelectric transducer is an MOS mold solid state camera according to claim 8 characterized by consisting of said semi-conductor substrate and said signal are recording field, and not preparing said punch-through prevention field directly under said signal are recording field.

[Claim 13] Said punch-through prevention field is an MOS mold solid state camera according to claim 12 characterized by adjoining said signal are recording field.

[Claim 14] The depth of said punch-through prevention field in said 2nd element field is an MOS mold solid state camera according to claim 1 characterized by being set as 0.2 micrometers or more 0.4 micrometers or less.

[Claim 15] It is the MOS mold solid state camera according to claim 1 characterized by setting the gate length of said 1st and 2nd MOS transistors as 0.4 micrometers or less, and setting the thickness of gate oxide as 10nm or less.

[Claim 16] The process which forms a discrete insulating layer on the semi-conductor substrate of the 1st conductivity type, and forms the 1st and the 2nd element field which were enclosed by said discrete insulating layer, The impurity of the 1st conductivity type is poured in into said semi-conductor substrate with ion-implantation. The process which forms the punch-through prevention field of the 1st conductivity type for preventing a punch-through at least in [whole] directly under [of said discrete insulating layer], and said 2nd element field, While forming the 1st MOS transistor for

reading the charge generated by the optoelectric transducer and said optoelectric transducer in said 1st element field The manufacture approach of the MOS mold solid state camera characterized by providing the process which forms the 2nd MOS transistor in said 2nd element field.

[Claim 17] Said impurity is the manufacture approach of the MOS mold solid state camera according to claim 16 which is the acceleration energy and the dose which run through said discrete insulating layer, and is characterized by being poured in into said semi-conductor substrate.

[Claim 18] Said impurity is the manufacture approach of the MOS mold solid state camera according to claim 16 characterized by using the mask at the time of the channel ion implantation which determines the threshold of said 2nd MOS transistor as it is, and being poured in into said semi-conductor substrate.

[Claim 19] Said impurity is the manufacture approach of the MOS mold solid state camera according to claim 16 characterized by pouring in a wrap resist layer into said semi-conductor substrate in it, using the part on said 1st element field as a mask.

[Claim 20] Said resist layer is the manufacture approach of the MOS mold solid state camera according to claim 19 which is a field inside the location where only constant width entered said 1st element field from said discrete insulating layer at least, and is characterized by being formed on the signal are recording field of the 2nd conductivity type of said optoelectric transducer.

[Claim 21] Said impurity is the manufacture approach of the MOS mold solid state camera according to claim 16 characterized by being poured also into the part in said 1st element field.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention] About the device structure of an MOS mold solid state camera, especially this invention has short gate length (channel length), and since gate oxide is thin, it is used for the MOS mold solid state camera which has an MOS transistor from which a punch-through poses a problem.

[0002]

[Description of the Prior Art] Drawing 10 shows the circuitry for 1 pixel of an MOS mold solid state camera.

[0003] A pixel consists of selector gates 25 for outputting the potential of the reset gate 23 for resetting the read-out gate 22 for transmitting the charge of the photodiode 21 for changing a lightwave signal into an electrical signal (charge), and a photodiode 21 to a detecting element (detection node) D, and the charge (potential) of a detecting element D, the magnification gate 24 which amplifies the potential of a detecting element D, and the selected pixel.

[0004] And the charge which photo electric conversion was carried out to a fixed period in the photodiode 21, and was accumulated in the signal are recording field is transmitted to a detecting element D via the read-out gate 22. The charge transmitted to the detecting element D changes the potential of a detecting element D from a photodiode 21. In order that the magnification gate 24 may amplify potential change of this detecting element D, the amplified signal potential is outputted from a pixel.

[0005] Here, in the MOS mold solid state camera, making high impurity concentration of a semi-conductor substrate (or well field) as thin as possible is further called for for the purpose of transmitting completely all the charges accumulated in the signal are recording field of a photodiode (photo-electric-conversion section) 21 to a detecting element D, stabilizing the property of the photodiode 21 in [all] a pixel, etc.

[0006] However, if an MOS transistor is made detailed for increase (densification of a pixel) of pixel capacity, the gate length (channel length) of an MOS transistor becomes short and the gate oxide becomes thin when the value of the high impurity concentration of a semi-conductor substrate (or well field) is low, regardless of a gate control, the punch-through that a charge flows from the source of an MOS transistor to a drain will occur.

[0007] When this punch-through occurs, an unnecessary signal (charge) will flow an MOS transistor and it becomes impossible to secure normal actuation of a solid state camera.

[0008] Then, it is necessary to prevent a punch-through. Conventionally, in the logic product, in order to prevent this punch-through, the punch-through prevention field is established in the interior of a semi-conductor substrate (location deep enough from a front face).

[0009] Since a punch-through prevention field is what prevents the source of an MOS transistor, and leak between drains, as for a punch-through prevention field, the source and the drain of p mold and an MOS transistor usually serve as p mold, when a semi-conductor substrate is n mold. And such a punch-through prevention field serves

as a means very effective in prevention of a punch-through to the logic product.

[0010] However, in an MOS mold solid state camera, it is necessary to form a photodiode in the interior of a semi-conductor substrate (location deep enough from a front face). Since a photodiode consists of for example, a p type semiconductor substrate and an n mold signal are recording field (impurity range), it must form this signal are recording field in the interior of a semi-conductor substrate (location deep enough from a front face).

[0011] In this case, if it is going to form a punch-through prevention field in a semi-conductor substrate, the conductivity type (for example, n mold) of the impurity (for example, Lynn) which constitutes the signal are recording field of a photodiode, and the conductivity type (for example, p) of the impurity (for example, boron) which constitutes a punch-through prevention field will become reverse mutually. And these signals are recording field and a punch-through prevention field are formed in the almost same location inside a semi-conductor substrate (location deep enough from a front face) as mentioned above.

[0012] Therefore, in case a signal are recording field will usually be formed since a signal are recording field will be formed in a punch-through prevention field after forming a punch-through prevention field if it is going to apply a punch-through prevention field to an MOS mold solid state camera, the impurity (for example, n mold impurity) of sufficient amount to reverse the conductivity type (for example, p mold) of a punch-through prevention field must be poured in.

[0013] By the way, in order to read completely all the charges accumulated in the signal are recording field of a photodiode by photo electric conversion, it becomes important to make depletion-ized potential of a photodiode as small as possible. In order to make depletion-ized potential of a photodiode small, it becomes effective to form the signal are recording field of a photodiode stably with the lowest possible high impurity concentration.

[0014] However, as mentioned above, when forming the signal are recording field of a photodiode in a punch-through prevention field, the impurity (for example, n mold impurity) of sufficient amount to reverse the conductivity type (for example, p mold) of a punch-through prevention field must be introduced in a semi-conductor substrate. It is necessary to pour in n mold impurity of high impurity concentration higher than p mold high impurity concentration of a punch-through prevention field into a semi-conductor substrate as an estimate simply.

[0015] In this case, if the point that the effect by p mold impurity and the effect by n mold impurity are offset mutually is taken into consideration, the high impurity

concentration of the signal are recording field of a photodiode will become equal to the value (dn-dp) which lengthened the high impurity concentration dp of p mold impurity which constitutes a punch-through prevention field from an amount dn of n mold impurities poured in into a semi-conductor substrate by the ion implantation in general.

[0016] However, the high impurity concentration dp of p mold impurity which constitutes the amount dn of n mold impurities and punch-through prevention field which are poured in into a semi-conductor substrate by the ion implantation serves as a both comparatively big numeric value. That is, since small fluctuation of a big numeric value turns into big fluctuation of a small numeric value when a big numeric value tends to be subtracted from a big numeric value and it is going to acquire a small numeric value, when a punch-through prevention field is applied to an MOS mold solid state camera, it becomes very difficult to make it thin, and for it to be stabilized and to obtain the high impurity concentration of the signal are recording field of a photodiode.

[0017] Small fluctuation of the high impurity concentration of n mold impurity poured in into a semi-conductor substrate by the ion implantation turns into big fluctuation of the high impurity concentration of the signal are recording field of a photodiode after all, and the depletion-ized potential of a photodiode is also changed sharply and it becomes impossible to read the charge of a signal are recording field stably in connection with this.

[0018]

[Problem(s) to be Solved by the Invention] Thus, in an MOS mold solid state camera, it originates in increase (densification of a pixel) of pixel capacity, and the gate length of an MOS transistor is short, the thickness of gate oxide becomes thin and a punch-through is posing a problem. It is very difficult by existence of the signal are recording field of a photodiode to, only already apply the punch-through prevention field put in practical use in the logic product etc. to an MOS mold solid state camera on the other hand.

[0019] Because, in order to ensure a transfer of a charge, it is desirable for it to be thin and to stabilize the high impurity concentration of the signal are recording field of a photodiode, and for it to be low and to stabilize the depletion-ized potential of a photodiode. However, it is because it becomes impossible to form a signal are recording field stably [are low high impurity concentration and] in order to have to reverse the conductivity type of this punch-through prevention field and to have to form a signal are recording field, if a punch-through prevention field is prepared.

[0020] That is, in the conventional MOS mold solid state camera, when an MOS transistor was made detailed, a punch-through became a problem and the

punch-through prevention field for punch-through prevention was prepared, it was difficult to be low and to stabilize the depletion-ized potential of a photodiode, and it was not able to manufacture stably an MOS mold solid state camera with uniform charge transfer capability.

[0021] This invention was made in order to solve the above-mentioned fault, and even if an MOS transistor is made detailed, the purpose is to propose the MOS mold solid state camera which can prevent a punch-through, and its manufacture approach, while it is low high impurity concentration and can form the signal are recording field of a photodiode stably.

[0022]

[Means for Solving the Problem] (1) The MOS mold solid state camera of this invention The 1st MOS transistor of the 2nd conductivity type for reading the optoelectric transducer formed in the semi-conductor substrate of the 1st conductivity type, and the charge which is formed in the 1st element field of said semi-conductor substrate, and is generated by said optoelectric transducer, It has the 2nd MOS transistor of the 2nd conductivity type formed in the 2nd element field of said semi-conductor substrate, and the punch-through prevention field of the 1st conductivity type for preventing a punch-through is established in said whole 2nd element field.

[0023] The MOS mold solid state camera of this invention is further equipped with the discrete insulating layer which encloses said the 1st and 2nd element field, and said punch-through prevention field is prepared also directly under said discrete insulating layer.

[0024] Said punch-through prevention field is established in the periphery of said 1st element field along with said discrete insulating layer.

[0025] The width of face from said discrete insulating layer to the edge of said punch-through prevention field in said 1st element field is secured more than the doubling gap of the mask material used in case said punch-through prevention field is formed. Said width of face is set as 0.2 micrometers or more.

[0026] The location of said punch-through prevention field in said 2nd element field is deeper than the location of said punch-through prevention field in directly under [of said discrete insulating layer].

[0027] The MOS mold solid state camera of this invention has two or more pixels, and each pixel has said optoelectric transducer, said 1st MOS transistor, and said 2nd MOS transistor.

[0028] Said optoelectric transducer is formed in said 1st element field, and the source of said 1st MOS transistor serves as a signal are recording field of the 2nd conductivity

type of said optoelectric transducer.

[0029] The MOS mold solid state camera of this invention is further equipped with the punch-through stopper of the 1st conductivity type formed directly under the drain of said 1st MOS transistor.

[0030] Said punch-through prevention field is prepared directly under the drain of said 1st MOS transistor. Moreover, said punch-through prevention field has covered the drain of said 1st MOS transistor, and a part of channel.

[0031] Said optoelectric transducer consists of said semi-conductor substrate and said signal are recording field, and said punch-through prevention field is not prepared directly under said signal are recording field.

[0032] Said punch-through prevention field adjoins said signal are recording field.

[0033] The depth of said punch-through prevention field in said 2nd element field is set as 0.2 micrometers or more 0.4 micrometers or less.

[0034] The gate length of said 1st and 2nd MOS transistors is set as 0.4 micrometers or less, and the thickness of gate oxide is set as 10nm or less.

[0035] (2) The manufacture approach of the MOS mold solid state camera of this invention The process which forms a discrete insulating layer on the semi-conductor substrate of the 1st conductivity type, and forms the 1st and the 2nd element field which were enclosed by said discrete insulating layer, The impurity of the 1st conductivity type is poured in into said semi-conductor substrate with ion-implantation. The process which forms the punch-through prevention field of the 1st conductivity type for preventing a punch-through at least in [whole] directly under [of said discrete insulating layer], and said 2nd element field, While forming the 1st MOS transistor for reading the charge generated by the optoelectric transducer and said optoelectric transducer in said 1st element field, it has the process which forms the 2nd MOS transistor in said 2nd element field.

[0036] Said impurity is the acceleration energy and the dose which run through said discrete insulating layer, and is poured in into said semi-conductor substrate.

[0037] The mask at the time of the channel ion implantation which determines the threshold of said 2nd MOS transistor is used for said impurity as it is, and it is poured in into said semi-conductor substrate.

[0038] Said impurity uses the part on said 1st element field as a mask, and a wrap resist layer is poured in into said semi-conductor substrate in it.

[0039] Said resist layer is a field inside the location where only constant width entered said 1st element field from said discrete insulating layer at least, and is formed on the signal are recording field of the 2nd conductivity type of said optoelectric transducer.

[0040] Said impurity is poured also into the part in said 1st element field.
[0041]
[Embodiment of the Invention] Hereafter, the MOS mold solid state camera and its manufacture approach of this invention are explained to a detail, referring to a drawing.
[0042] [Gestalt of the 1st operation] drawing 1 shows the device structure of the MOS mold solid state camera in connection with the gestalt of the 1st operation of this invention.
[0043] The p type semiconductor substrate 1 is the low high impurity concentration 3, for example, 1x1015 atoms/cm. It has. The semi-conductor substrate 1 serves as an anode of a photodiode, for example, the semi-conductor substrate 1 is set as touch-down potential. However, p mold well field is formed in the semi-conductor substrate 1, and it is good also considering this p mold well field as an anode of a photodiode. In this case, the high impurity concentration of p mold well field is 1x1015 atoms/cm3. It is set up.
[0044] On the semi-conductor substrate 1, the discrete insulating layer 10 which separates components electrically is arranged. this example -- a discrete insulating layer 10 -- for example, LOCOS (Local Oxidation ofSilicon) -- although it is the field oxide formed of law -- this -- replacing with -- for example, STI (Shallow Trench Isolation) -- the oxide film formed of law may be used.
[0045] The component field A enclosed by the discrete insulating layer 10 is the field in which it reads with the photodiode 21 shown in drawing 10 , and the gate 22 is formed. Moreover, the component field B enclosed by the discrete insulating layer 10 is the field in which components (a photodiode 21 and components other than read-out gate 22), such as the reset gate 23 shown in drawing 10 , the magnification gate 24, and a selector gate 25, are formed.
[0046] It sets to the component field A and is n- in the interior of the semi-conductor substrate 1 (location deep enough from a front face). The mold signal are recording field 2 is arranged. Moreover, at this example, it is n-. The mold signal are recording field 2 is p+. It is directly formed in the semi-conductor substrate 1, without being formed in the mold punch-through prevention field 6. n- In the mold signal are recording field 2, the p++ mold surface shielding layer 3 is arranged.
[0047] Moreover, in the component field A, it is the interior of the semi-conductor substrate 1 (location deep enough from a front face), and is n-. p+ mold punch-through stopper 5 is arranged at a different part from the part by which the mold signal are recording field 2 is arranged. p+ In the mold punch-through stopper 5, the n type 1st semiconductor region 4 is arranged.
[0048] n- p mold read-out channel field 9 top between the mold signal are recording field

2, and the n type 1st semiconductor region 4 -- for example, SiO2 from -- the read-out gate electrode 8 is arranged via the gate oxide 7 constituted. The read-out gate electrode 8 consists of conductive polish recon film containing for example, n mold impurity. The read-out gate electrode 8 is a gate electrode of the read-out gate 22 of drawing 1010 .

[0049] p+ for preventing a punch-through in the component field B inside the semi-conductor substrate 1 (location deep enough from a front face) The mold punch-through prevention field 6 is arranged. p+ The mold punch-through prevention field 6 is arranged to the whole component field B. In p+ mold punch-through prevention field 6, the n type 2nd semiconductor region 11 and, and the n type 3rd semiconductor region 12 are arranged.

[0050] p mold channel field 13 top between the n type 2nd semiconductor region 11, and the n type 3rd semiconductor region 12 -- for example, SiO2 from -- the gate electrode 14 is arranged via the gate oxide 7 constituted. The gate electrode 14 consists of conductive polish recon film containing for example, n mold impurity. The gate electrode 14 turns into a gate electrode of MOS transistors, such as the reset gate 23 of drawing 10 , the magnification gate 24, and a selector gate 25.

[0051] The description of the device structure of an above-mentioned MOS mold solid state camera is p+ in the first place. The mold punch-through prevention field 6 is n-. It is in the point which is not formed directly under the mold signal are recording field 2. That is, at this invention, it is n-. It is directly formed in the semi-conductor substrate 1, and the mold signal are recording field 2 is p+. Since it is not formed in the mold punch-through prevention field 6, it is n-. It is low high impurity concentration, and the mold signal are recording field 2 can be formed stably.

[0052] Specifically, the high impurity concentration (for example, boron concentration) of the semi-conductor substrate 1 is 1x1015 atoms/cm3 as mentioned above. It is set up and is p+. The high impurity concentration (for example, boron concentration) of the mold punch-through prevention field 6 is 1x1017 atoms/cm3. It is set up.

[0053] That is, at this invention, it is p+. In the semi-conductor substrate 1 which has high impurity concentration also with double figures smaller than the high impurity concentration of the mold punch-through prevention field 6, it is n-. Since the mold signal are recording field 2 will be formed, the dose by the ion implantation of n mold impurity can be set up low, and it is n- as a result. It is low high impurity concentration, and the mold signal are recording field 2 can be stably formed now.

[0054] To the second, it is p+. Although formed in directly under [of a discrete insulating layer 10], and the whole component field B, it sets to the component field A, and the mold punch-through prevention field 6 is p+ only directly under the n type 1st

semiconductor region 4. The mold punch-through stopper 5 is formed. That is, the n type 1st semiconductor region 4 does not need to serve as the detecting element (detection node) D shown in drawing 10 , and does not need to set up the high impurity concentration low like n-mold signal are recording field 2.

[0055] Therefore, directly under the n type 1st semiconductor region 4, it is p+. It is necessary to prevent the punch-through which forms the mold punch-through stopper 5, for example, is produced between the n type 1st semiconductor region 4, and other n-type-semiconductor fields.

[0056] In addition, p+ The mold punch-through prevention field 6 needs to be certainly formed directly under a discrete insulating layer 10. It is for preventing effectively the punch-through between two n-type-semiconductor fields whose discrete insulating layers 10 are pinched.

[0057] For this reason, p+ After forming a discrete insulating layer 10, before the mold punch-through prevention field 6 forms the gate electrodes 8 and 14, it is formed by predetermined acceleration energy and the ion-implantation of a predetermined dose. In the component field B to which a discrete insulating layer 10 does not exist as they are shown in drawing 1 , when the conditions of the ion implantation at this time are set as conditions on which an impurity (for example, boron) runs through a discrete insulating layer 10, an impurity reaches to the deep location of the semi-conductor substrate 1, and it is p+. The mold punch-through prevention field 6 is formed in a location deep enough from the front face of the semi-conductor substrate 1.

[0058] In addition, in drawing 1 , the thickness of gate oxide 7 is set as about 8nm, and the gate length (channel length) of the gate electrode 14 is set as about 0.4 micrometers. Moreover, the high impurity concentration of the p++ mold surface shielding layer 3 is 1x1018 atoms/cm3. It is set as extent and is p+. The mold punch-through stopper 5 and p+ Both the high impurity concentration of the mold punch-through prevention field 6 is 1x1017 atoms/cm3, for example. It is set as extent.

[0059] As mentioned above, as explained, while according to the MOS mold solid state camera in connection with the gestalt of the 1st operation of this invention being low high impurity concentration and being able to form the signal are recording field of a photodiode stably, a punch-through can also be prevented even if an MOS transistor is made detailed.

[0060] The MOS mold solid state camera in connection with the gestalt of [gestalt of the 2nd operation] book operation is p+. It has the description to the mold punch-through prevention field 6.

[0061] In the MOS mold solid state camera in connection with the gestalt of the 1st

above-mentioned operation, a photodiode is formed in the source side of the read-out gate (MOS transistor of the component field A), and the n type 1st semiconductor region 4 as a detecting element (detection node) D is arranged at the drain side. And it is p+ directly under this the n type 1st semiconductor region 4. The mold punch-through stopper 5 is p+. It is formed independently [the mold punch-through prevention field 6].
[0062] However, p+ The mold punch-through stopper 5 and p+ The mold punch-through prevention field 6 is the same purpose (punch-through prevention) mutually, and is mutually formed with the same high impurity concentration. Therefore, directly under the n type 1st semiconductor region 4, it is p+. Not the mold punch-through stopper 5 but p+ It cannot be overemphasized that the mold punch-through prevention field 6 may be formed.
[0063] So, at the gestalt of this operation, it is p+ also directly under the n type 1st semiconductor region 4. The mold punch-through prevention field 6 is formed. Consequently, at the gestalt of this operation, it is p+. The mold punch-through stopper 5 becomes unnecessary, and only the part can acquire the effectiveness that a production process is simplified.
[0064] Hereafter, the MOS mold solid state camera in connection with the gestalt of this operation is explained.
[0065] Drawing 2 shows the device structure of the MOS mold solid state camera in connection with the gestalt of the 2nd operation of this invention.
[0066] The p type semiconductor substrate 1 is the low high impurity concentration 3, for example, 1x1015 atoms/cm. It has. The semi-conductor substrate 1 serves as an anode of a photodiode, for example, the semi-conductor substrate 1 is set as touch-down potential. However, p mold well field is formed in the semi-conductor substrate 1, and it is good also considering this p mold well field as an anode of a photodiode. In this case, the high impurity concentration of p mold well field is 1x1015 atoms/cm3. It is set up.
[0067] On the semi-conductor substrate 1, the discrete insulating layer 10 which separates components electrically is arranged. this example -- a discrete insulating layer 10 -- for example, LOCOS (Local Oxidation ofSilicon) -- although it is the field oxide formed of law -- this -- replacing with -- for example, STI (Shallow Trench Isolation) -- the oxide film formed of law may be used.
[0068] The component field A enclosed by the discrete insulating layer 10 is the field in which it reads with the photodiode 21 shown in drawing 10 , and the gate 22 is formed. Moreover, the component field B enclosed by the discrete insulating layer 10 is the field in which components (a photodiode 21 and components other than read-out gate 22), such as the reset gate 23 shown in drawing 10 , the magnification gate 24, and a selector

gate 25, are formed.

[0069] It sets to the component field A and is n- in the interior of the semi-conductor substrate 1 (location deep enough from a front face). The mold signal are recording field 2 is arranged. Moreover, at this example, it is n-. The mold signal are recording field 2 is p+. It is directly formed in the semi-conductor substrate 1, without being formed in the mold punch-through prevention field 6. n- In the mold signal are recording field 2, the p++ mold surface shielding layer 3 is arranged.

[0070] Moreover, in the component field A, it is the interior of the semi-conductor substrate 1 (location deep enough from a front face), and is n-. p+ mold punch-through prevention field 6 is arranged at a different part from the part by which the mold signal are recording field 2 is arranged. p+ In the mold punch-through prevention field 6, the n type 1st semiconductor region 4 is arranged.

[0071] n- p mold read-out channel field 9 top between the mold signal are recording field 2, and the n type 1st semiconductor region 4 -- for example, SiO2 from -- the read-out gate electrode 8 is arranged via the gate oxide 7 constituted. The read-out gate electrode 8 consists of conductive polish recon film containing for example, n mold impurity. The read-out gate electrode 8 is a gate electrode of the read-out gate 22 of drawing 1010 .

[0072] p+ for preventing a punch-through in the component field B inside the semi-conductor substrate 1 (location deep enough from a front face) The mold punch-through prevention field 6 is arranged. p+ The mold punch-through prevention field 6 is arranged to the whole component field B. In p+ mold punch-through prevention field 6, the n type 2nd semiconductor region 11 and, and the n type 3rd semiconductor region 12 are arranged.

[0073] p mold channel field 13 top between the n type 2nd semiconductor region 11, and the n type 3rd semiconductor region 12 -- for example, SiO2 from -- the gate electrode 14 is arranged via the gate oxide 7 constituted. The gate electrode 14 consists of conductive polish recon film containing for example, n mold impurity. The gate electrode 14 turns into a gate electrode of MOS transistors, such as the reset gate 23 of drawing 10 , the magnification gate 24, and a selector gate 25.

[0074] It is p+ like the MOS mold solid state camera on the device structure of an above-mentioned MOS mold solid state camera, and in connection with the gestalt of the 1st above-mentioned operation. The mold punch-through prevention field 6 is n-. It is not formed directly under the mold signal are recording field 2. That is, at this invention, it is directly formed in the semi-conductor substrate 1, and n-mold signal are recording field 2 is p+. Since it is not formed in the mold punch-through prevention field 6, it is n-. It is low high impurity concentration, and the mold signal are recording field 2

can be formed stably.

[0075] Specifically, the high impurity concentration (for example, boron concentration) of the semi-conductor substrate 1 is 1x1015 atoms/cm3 as mentioned above. It is set up and is p+. The high impurity concentration (for example, boron concentration) of the mold punch-through prevention field 6 is 1x1017 atoms/cm3. It is set up.

[0076] That is, at this invention, it is p+. In the semi-conductor substrate 1 which has high impurity concentration also with double figures smaller than the high impurity concentration of the mold punch-through prevention field 6, it is n-. Since the mold signal are recording field 2 will be formed, the dose by the ion implantation of n mold impurity can be set up low, and it is n- as a result. It is low high impurity concentration, and the mold signal are recording field 2 can be stably formed now.

[0077] In addition, p+ The mold punch-through prevention field 6 needs to be certainly formed directly under a discrete insulating layer 10. It is for preventing effectively the punch-through between two n-type-semiconductor fields whose discrete insulating layers 10 are pinched.

[0078] For this reason, p+ After forming a discrete insulating layer 10, before the mold punch-through prevention field 6 forms the gate electrodes 8 and 14, it is formed by predetermined acceleration energy and the ion-implantation of a predetermined dose. In the component field to which a discrete insulating layer 10 does not exist as they are shown in drawing 2 , when the conditions of the ion implantation at this time are set as conditions on which an impurity (for example, boron) runs through a discrete insulating layer 10, an impurity reaches to the deep location of the semi-conductor substrate 1, and it is p+. The mold punch-through prevention field 6 is formed in a location deep enough from the front face of the semi-conductor substrate 1.

[0079] In addition, in drawing 2 , the thickness of gate oxide 7 is set as about 8nm, and the gate length (channel length) of the gate electrode 14 is set as about 0.4 micrometers. Moreover, the high impurity concentration of the p++ mold surface shielding layer 3 is 1x1018 atoms/cm3. It is set as extent and is p+. The mold punch-through stopper 5 and p+ Both the high impurity concentration of the mold punch-through prevention field 6 is 1x1017 atoms/cm3, for example. It is set as extent.

[0080] As mentioned above, as explained, while according to the MOS mold solid state camera in connection with the gestalt of the 2nd operation of this invention being low high impurity concentration and being able to form the signal are recording field of a photodiode stably, a punch-through can also be prevented even if an MOS transistor is made detailed.

[0081] The MOS mold solid state camera in connection with the gestalt of [gestalt of the

3rd operation] book operation is also p+. It has the description to the mold punch-through prevention field 6.

[0082] With the MOS mold solid state camera in connection with the gestalt of the 2nd above-mentioned operation, it is p+ also directly under the n type 1st semiconductor region 4 by the side of the drain of the read-out gate (MOS transistor of the component field A). The mold punch-through prevention field 6 is formed.

[0083] On the other hand, at the gestalt of this operation, it is p+. In the component field A, the mold punch-through prevention field 6 is formed so that not only directly under [of the n type 1st semiconductor region 4] but a part of read-out gate (MOS transistor) of the channel of read-out gate electrode 8 directly under may be covered.

[0084] Thus, p+ It is easily realizable to form the mold punch-through prevention field 6 in a part of channel of directly under [of the n type 1st semiconductor region 4] and the read-out gate only by transforming the mask pattern at the time of an ion implantation.

[0085] Hereafter, the MOS mold solid state camera in connection with the gestalt of this operation is explained.

[0086] Drawing 3 shows the device structure of the MOS mold solid state camera in connection with the gestalt of the 3rd operation of this invention.

[0087] The p type semiconductor substrate 1 is the low high impurity concentration 3, for example, 1x1015 atoms/cm. It has. The semi-conductor substrate 1 serves as an anode of a photodiode, for example, the semi-conductor substrate 1 is set as touch-down potential. However, p mold well field is formed in the semi-conductor substrate 1, and it is good also considering this p mold well field as an anode of a photodiode. In this case, the high impurity concentration of p mold well field is 1x1015 atoms/cm3. It is set up.

[0088] On the semi-conductor substrate 1, the discrete insulating layer 10 which separates components electrically is arranged. this example -- a discrete insulating layer 10 -- for example, LOCOS (Local Oxidation ofSilicon) -- although it is the field oxide formed of law -- this -- replacing with -- for example, STI (Shallow Trench Isolation) -- the oxide film formed of law may be used.

[0089] The component field A enclosed by the discrete insulating layer 10 is the field in which it reads with the photodiode 21 shown in drawing 10 , and the gate 22 is formed. Moreover, the component field B enclosed by the discrete insulating layer 10 is the field in which components (a photodiode 21 and components other than read-out gate 22), such as the reset gate 23 shown in drawing 10 , the magnification gate 24, and a selector gate 25, are formed.

[0090] It sets to the component field A and is n- in the interior of the semi-conductor substrate 1 (location deep enough from a front face). The mold signal are recording field

2 is arranged. Moreover, at this example, it is n-. The mold signal are recording field 2 is p+. It is directly formed in the semi-conductor substrate 1, without being formed in the mold punch-through prevention field 6. n- In the mold signal are recording field 2, the p++ mold surface shielding layer 3 is arranged.

[0091] Moreover, in the component field A, it is the interior of the semi-conductor substrate 1 (location deep enough from a front face), and is n-. To a different part (a part of read-out channel field 9 of the read-out gate is included), the part by which the mold signal are recording field 2 is arranged is p+. The mold punch-through prevention field 6 is arranged. p+ In the mold punch-through prevention field 6, the n type 1st semiconductor region 4 is arranged.

[0092] n- p mold read-out channel field 9 top between the mold signal are recording field 2, and the n type 1st semiconductor region 4 -- for example, SiO2 from -- the read-out gate electrode 8 is arranged via the gate oxide 7 constituted. The read-out gate electrode 8 consists of conductive polish recon film containing for example, n mold impurity. The read-out gate electrode 8 is a gate electrode of the read-out gate 22 of drawing 1010 .

[0093] p+ for preventing a punch-through in the component field B inside the semi-conductor substrate 1 (location deep enough from a front face) The mold punch-through prevention field 6 is arranged. p+ The mold punch-through prevention field 6 is arranged to the whole component field B. In p+ mold punch-through prevention field 6, the n type 2nd semiconductor region 11 and, and the n type 3rd semiconductor region 12 are arranged.

[0094] p mold channel field 13 top between the n type 2nd semiconductor region 11, and the n type 3rd semiconductor region 12 -- for example, SiO2 from -- the gate electrode 14 is arranged via the gate oxide 7 constituted. The gate electrode 14 consists of conductive polish recon film containing for example, n mold impurity. The gate electrode 14 turns into a gate electrode of MOS transistors, such as the reset gate 23 of drawing 10 , the magnification gate 24, and a selector gate 25.

[0095] It is p+ like the MOS mold solid state camera on the device structure of an above-mentioned MOS mold solid state camera, and in connection with the gestalt of the 1st and 2nd above-mentioned operations. The mold punch-through prevention field 6 is n-. It is not formed directly under the mold signal are recording field 2. That is, at this invention, it is n-. It is directly formed in the semi-conductor substrate 1, and the mold signal are recording field 2 is p+. Since it is not formed in the mold punch-through prevention field 6, it is n-. It is low high impurity concentration, and the mold signal are recording field 2 can be formed stably.

[0096] Specifically, the high impurity concentration (for example, boron concentration)

of the semi-conductor substrate 1 is 1x1015 atoms/cm3 as mentioned above. It is set up and is p+. The high impurity concentration (for example, boron concentration) of the mold punch-through prevention field 6 is 1x1017 atoms/cm3. It is set up.

[0097] That is, at this invention, it is p+. In the semi-conductor substrate 1 which has high impurity concentration also with double figures smaller than the high impurity concentration of the mold punch-through prevention field 6, it is n-. Since the mold signal are recording field 2 will be formed, the dose by the ion implantation of n mold impurity can be set up low, and it is n- as a result. It is low high impurity concentration, and the mold signal are recording field 2 can be stably formed now.

[0098] In addition, p+ The mold punch-through prevention field 6 needs to be certainly formed directly under a discrete insulating layer 10. It is for preventing effectively the punch-through between two n-type-semiconductor fields whose discrete insulating layers 10 are pinched.

[0099] For this reason, p+ After forming a discrete insulating layer 10, before the mold punch-through prevention field 6 forms the gate electrodes 8 and 14, it is formed by predetermined acceleration energy and the ion-implantation of a predetermined dose. In the component field to which a discrete insulating layer 10 does not exist as they are shown in drawing 3 , when the conditions of the ion implantation at this time are set as conditions on which an impurity (for example, boron) runs through a discrete insulating layer 10, an impurity reaches to the deep location of the semi-conductor substrate 1, and it is p+. The mold punch-through prevention field 6 is formed in a location deep enough from the front face of the semi-conductor substrate 1.

[0100] In addition, in drawing 3 , the thickness of gate oxide 7 is set as about 8nm, and the gate length (channel length) of the gate electrode 14 is set as about 0.4 micrometers. Moreover, the high impurity concentration of the p++ mold surface shielding layer 3 is 1x1018 atoms/cm3. It is set as extent and is p+. The mold punch-through stopper 5 and p+ Both the high impurity concentration of the mold punch-through prevention field 6 is 1x1017 atoms/cm3, for example. It is set as extent.

[0101] As mentioned above, as explained, while according to the MOS mold solid state camera in connection with the gestalt of the 3rd operation of this invention being low high impurity concentration and being able to form the signal are recording field of a photodiode stably, a punch-through can also be prevented even if an MOS transistor is made detailed.

[0102] [Explanation of the manufacture approach], next the manufacture approach of the MOS mold solid state camera of this invention are explained. In addition, the following explanation is applicable to all the manufacture approaches of the MOS mold

solid state camera in connection with the gestalt of the above-mentioned 1st thru/or the 3rd above-mentioned operation. It will explain about a step original with the gestalt of each operation each time.

[0103] first, it is shown in drawing 4 -- as -- LOCOS -- a discrete insulating layer 10 is formed on the p-type semiconductor substrate 1 by law. Then, the buffer oxide film 15 is formed on the component fields A and B enclosed by the discrete insulating layer 10 by thermal oxidation.

[0104] Next, as shown in drawing 5 , the so-called channel ion implantation for determining the threshold of an MOS transistor is performed to the component field A, and p mold read-out channel field 9 is formed. Similarly the so-called channel ion implantation for determining the threshold of an MOS transistor is performed to the component field B, and p mold channel field 13 is formed.

[0105] In this example, both the channel fields 9 and 13 are formed like 2 times of ion grouting. In this case, in order to form both the channel fields 9 and 13, 2 times of PEPs (Photo Engraving Process) are needed. However, when setting up mutually the threshold of the MOS transistor formed in the component fields A and B similarly, both the channel fields 9 and 13 can be formed like 1 time of ion grouting. In this case, PEP for forming both the channel fields 9 and 13 is good at once.

[0106] Then, the resist layer 16 is formed and the resist pattern (resist layer 16) as a mask is made to remain on the component field A by PEP.

[0107] In addition, if the resist layer 16 is covered for the whole component field A at this time, it will become the manufacture approach of the device in connection with the gestalt of the 1st above-mentioned operation. Moreover, if the resist layer 16 is made not to be arranged at the part on the component field A, it will become the manufacture approach of the device in connection with the gestalt of the 2nd and 3rd above-mentioned operations.

[0108] And if the resist layer 16 is used as a mask and the ion implantation of the p mold impurity (for example, boron) is carried out with ion-implantation, in the interior of the semi-conductor substrate 1, it will be p+. The mold punch-through prevention field 6 is formed.

[0109] At this time, it is p+. The acceleration energy at the time of an ion implantation is set up so that the mold punch-through prevention field 6 may be formed in the location of 0.2-0.4 micrometers from the front face of the semi-conductor substrate 1. As [form / directly under a discrete insulating layer 10 / naturally / however, / as for this condition / p+ mold punch-through prevention field 6]

[0110] Moreover, p+ The high impurity concentration of the mold punch-through

prevention field 6 is 1x1017 atoms/cm3. The dose at the time of an ion implantation is set up so that it may become extent. At this example, it is p+. The ion implantation for forming the mold punch-through prevention field 6 is p+ by two ion implantations or more, although premised on being 1 time. You may make it form the mold punch-through prevention field 6.

[0111] Here, the delicate conditions which can respond to an actual product are explained. Namely, p+ In forming the mold punch-through prevention field 6, in practice, rather than the size of the component field A, it turns around the resist layer 16 one, and it is set as small size. The reason is p+. It is because it can prevent that the depletion layer of a photodiode reaches the damage by which the mold punch-through prevention field 6 will be formed in a discrete insulating layer 10 if it is made only for a few to enter the component field A in the circumference of the component field A.

[0112] In addition, p+ As for the width of face X to which the mold punch-through prevention field 6 enters the component field A, it is desirable to set up in consideration of a doubling gap of a mask (resist layer 16) more than the doubling gap. For example, the width of face X is set as about 0.2 micrometers or the value beyond it.

[0113] Then, the buffer oxide film 15 on the component field B is removed, and the thickness 7 of 10nm or less, for example, about 8nm gate oxide, is further formed on the component field B by the oxidizing [thermally] method. Then, the resist layer 16 on the component field A is removed, and the buffer oxide film 15 on the component field A is removed further.

[0114] Next, as shown in drawing 6 , the thickness 7 of 10nm or less, for example, about 8nm gate oxide, is formed on the component field A by the oxidizing [thermally] method.

[0115] In addition, although the gate oxide 7 of the component field A and the gate oxide 7 of the component field B were formed by different step in this example, naturally you may form by the same step. In this case, after removing the resist layer 16 of drawing 5 , the buffer oxide film 15 on the component fields A and B is removed by coincidence, and gate oxide 7 is formed on the component fields A and B at coincidence.

[0116] Then, if it goes via a step called formation of the conductive polish recon film containing an impurity, formation of a resist layer, and PEP and RIE, the read-out gate electrode 8 will be formed on the gate oxide 7 of the component field A, and the gate electrode 14 will be formed on the gate oxide 7 of the component field B.

[0117] Moreover, **** of a step called formation of an oxide film (or nitride) and RIE forms the so-called sidewall (spacer) in the side attachment wall of the gate electrodes 8 and 14.

[0118] Then, about the manufacture approach of the device in connection with the gestalt of the 1st above-mentioned operation, as shown in drawing 6 , the resist pattern (resist layer 17) which has opening is formed in the part on the component field A by spreading and PEP of a resist layer. And with ion-implantation, the resist layer 17 is used as a mask, p mold impurity (for example, boron) is poured in into the semi-conductor substrate 1, and it is p+. The mold punch-through stopper 5 is formed. Then, the resist layer 17 is removed.

[0119] In addition, it is related with the manufacture approach of the device in connection with the gestalt of the 2nd and 3rd above-mentioned operations, and, naturally is p+. About the step which forms the mold punch-through stopper 5, it is unnecessary.

[0120] Next, as shown in drawing 7 , the resist pattern (resist layer 18) which has opening is formed in the field which forms the photodiode on the component field A by spreading and PEP of a resist layer. And with ion-implantation, the resist layer 18 and a sidewall are used as a mask, in the semi-conductor substrate 1, p mold impurity (for example, BF2) is poured in, and the p++ mold surface shielding layer 3 is formed. Then, the resist layer 18 is removed.

[0121] Next, as shown in drawing 8 , the sidewall which exists in the side attachment wall of the gate electrodes 8 and 14 is removed. And the resist pattern (resist layer 18') which has opening is again formed in the field which forms the photodiode on the component field A by spreading and PEP of a resist layer. Then, with ion-implantation, resist layer 18' is used as a mask, n mold impurity (for example, Lynn) is poured in into the semi-conductor substrate 1, and it is n-. The mold signal are recording field 2 is formed.

[0122] Then, resist layer 18' is removed.

[0123] Finally, as shown in drawing 9 , the resist pattern (resist layer 19) which has opening is formed on the part on the component field A, and the component field B by spreading and PEP of a resist layer. Then, with ion-implantation, the resist layer 19 and the gate electrodes 9 and 14 are used as a mask, in the semi-conductor substrate 1, n mold impurity (for example, Lynn) is poured in, and the n type 1st thru/or the 3rd semiconductor region 4, 11, and 12 are formed.

[0124] Then, the resist layer 19 is removed.

[0125] In addition, although a wiring process, a passivation process, etc. are performed after this, it omits about it.

[0126] As mentioned above, the MOS mold solid state camera in connection with this invention is completed.

[0127] [Others] It sets to the MOS mold solid state camera in connection with the gestalt of the 1st above-mentioned operation, and is p+. The mold punch-through stopper 5 may be omitted. In this case, p+ The step (see the explanation of the manufacture approach) which forms the mold punch-through stopper 5 is skipped, and it can contribute to reduction of a manufacturing cost. Moreover, it is not based on the MOS mold solid state camera in connection with the gestalt of the 2nd and 3rd operations, but ** is also p+. If only constant width X makes the mold punch-through prevention field 6 enter the component field A (refer to drawing 5), also in the MOS transistor of the component field A, the effectiveness of punch-through prevention can fully be acquired.

[0128] In the MOS mold solid state camera in connection with the gestalt of the above-mentioned 1st thru/or the 3rd above-mentioned operation, p+ mold punch-through prevention field 6 may be formed by the ion implantation of p mold impurity, using the mask used at the time of the ion implantation for determining the threshold of an MOS transistor as it is. To the channel section of the read-out gate in the component field A (MOS transistor), this modification is applied, when not performing a channel ion implantation.

[0129] In the MOS mold solid state camera in connection with the gestalt of the above-mentioned 1st thru/or the 3rd above-mentioned operation, although it was the example in which the n channel MOS transistor was formed in the p type semiconductor substrate, this invention can be applied, for example, also when forming a p channel MOS transistor in a n-type-semiconductor substrate.

[0130]

[Effect of the Invention] As mentioned above, according to [as explained] the MOS mold solid state camera and its manufacture approach of this invention, directly under [signal are recording field] a photodiode, it is p+. The mold punch-through prevention field is not formed. On the other hand, it is p+. Only constant width enters at least the component field in which the read-out gate (MOS transistor) where the source serves as a signal are recording field of a photodiode is formed, and a mold punch-through prevention field is formed in the whole component field other than the component field.

[0131] Therefore, when the gate length of an MOS transistor becomes short and the thickness of the gate oxide becomes thin, it becomes possible to prevent both the punch-through of an MOS transistor, and the punch-through between components (between two components whose discrete insulating layers are pinched). Moreover, it is the signal are recording field of a photodiode p+ Since it is not necessary to reverse the conductivity type of a mold punch-through prevention field, and to form, it can be low

and the depletion-ized potential of the photodiode formed in a single pixel can be stabilized.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] The sectional view showing the MOS mold solid state camera in connection with the gestalt of the 1st operation of this invention.
[Drawing 2] The sectional view showing the MOS mold solid state camera in connection with the gestalt of the 2nd operation of this invention.
[Drawing 3] The sectional view showing the MOS mold solid state camera in connection with the gestalt of the 3rd operation of this invention.
[Drawing 4] The sectional view showing one process of the manufacture approach of the MOS mold solid state camera in connection with this invention.
[Drawing 5] The sectional view showing one process of the manufacture approach of the MOS mold solid state camera in connection with this invention.
[Drawing 6] The sectional view showing one process of the manufacture approach of the MOS mold solid state camera in connection with this invention.
[Drawing 7] The sectional view showing one process of the manufacture approach of the MOS mold solid state camera in connection with this invention.
[Drawing 8] The sectional view showing one process of the manufacture approach of the MOS mold solid state camera in connection with this invention.
[Drawing 9] The sectional view showing one process of the manufacture approach of the MOS mold solid state camera in connection with this invention.
[Drawing 10] The circuit diagram showing the pixel of an MOS mold solid state camera.
[Description of Notations]
1 [ ] : -- P Type Semiconductor Substrate,
2 [ ] :N- Mold Signal Are Recording Field,
3 [ ] : -- P++ Mold Surface Shielding Layer,
4 [ ] : -- N Type 1st Semiconductor Region,
5 [ ] :P+ Mold Punch-through Stopper,
6 [ ] :P+ Mold Punch-through Prevention Field,
7 [ ] : -- Gate Oxide,

8 [ ] : -- Read-out Gate Electrode,
9 [ ] : -- P Mold Read-out Channel Field,
10 [ ] : -- Discrete Insulating Layer,
11 [ ] : -- N Type 2nd Semiconductor Region,
12 [ ] : -- N Type 3rd Semiconductor Region,
13 [ ] : -- P Mold Channel Field,
14 [ ] : -- Gate Electrode,
15 [ ] : -- Buffer Oxide Film,
16, 17, 18, 18', 19 : Resist layer,
21 [ ] : -- Photodiode,
22 [ ] : -- Read-out Gate,
23 [ ] : -- Reset Gate,
24 [ ] : -- Magnification Gate,
25 [ ] : -- Selector Gate,
26 [ ] : -- Vertical-Scanning Circuit,
27 [ ] : -- Horizontal Scanning Circuit,
28 [ ] : -- the load gate.

[Translation done.]